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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,384	09/30/2003	Li-Jau Yang	CISCO-8091	9157

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SIERRA PATENT GROUP, LTD.
1657 Hwy 395, Suite 202
Minden, NV 89423

EXAMINER	
PALIWAL, YOGESH	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,384	YANG ET AL.	
	Examiner	Art Unit	
	Yogesh Paliwal	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *3, 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-12, 14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/1/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species 1 in the reply filed on 2/28/2007 is acknowledged.

Claims 3 and 13 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species 2, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 2/28/2007.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim a of copending Application No. 10/676390. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the limitation of claim 1 except following limitations are anticipated by claim 1 of application number 10/676390:

a crypto communications module coupled to said crypto engine;

and said PHY communications module being operatively coupled to said crypto communications module.

Fujimori et al. (US 2004/0030805 A1) teaches a crypto communications module coupled to a crypto engine **(Fig. 7, Numeral 326, data link and other links that are connected to component 326 providing data and control signals)**; and a PHY communications module being operatively coupled to a crypto communications module **(Fig. 7, encoder/scrambler is residing within PHY and sharing control signals with other components of PHY).**t would have been obvious to modify claim 1 of application 10/676390 to include crypto communications module coupled to crypto engine, as taught by Fujimori to provide control and data signal to crypto engine so that crypto engine can perform cryptographic operations on data. Further it would have been obvious to couple crypto communication module to the PHY communication module so that data can be transferred to the medium through PHY after cryptographic operation is completed.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections - 37 CFR 1.75(a)

3. The following is a quotation of 37 CFR 1.75(a):

> The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.

Claim 1 is objected to under 37 CFR 1.75(a), as failing to particularly point out and distinctly claim the subject matter which application regards as his invention or discovery.

Claim 1 recite, "said digital circuitry configured to transmit to, and receive from, a Media Access Controller".

However, it is not clear from the claim what is mend by "configured to transmit to, and receive from, a Media Access Controller"?

In light of the corresponding written description of the invention, and for purposes of examination, the following interpretation of claim 1, lines 5-6 will be assumed: digital circuitry coupled to said analog circuitry, said digital circuitry configured to transmit to, and receive data/control signals (as depicted in Fig. 3) from, a Media Access Controller (MAC). Correction is required.

Claim Objections - 37 CFR 1.75(d)(1)

4. The following is a quotation of 37 CFR 1.75(d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

Claims **7-10 and 17-20** are objected to under 37 CFR 1.75(d)(1), as failing to conform to the invention as set forth in the remainder of the specification.

Claims 7-10 and 17-20 are objected because specification failed to provide proper antecedent basis for the claimed subject matter. See MPEP § 608.01(o). The examiner suggests adding claim limitations back to the specification without adding new matter. Correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **1-2, 4-12, 14-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Fujimori et al. (US 2004/0030805 A1).

Regarding **Claim 1**, Fujimori discloses an apparatus for providing link layer security in a Physical Layer Transceiver (PHY) comprising:

analog circuitry configured to transmit to, and receive data from, a data transmission medium **(Fig. 4, Numerals 1, 17 and 30 and paragraph 0030)**

digital circuitry coupled to said analog circuitry **(Fig. 5, Numeral 130)**, said digital circuitry configured to transmit to, and receive data/control signals [as explained in 37 CFR 1.75(d)(1) objection above] from, a Media Access Controller (MAC) **(Fig. 5, numerals 20 and 10)**

a PHY communications module coupled to said analog and digital circuitry **(Fig. 4, Numerals 15 and 17);**

a crypto engine coupled to said digital circuitry **(Fig. 7, Numeral 326, "Encoder/Scrambler")**;

a crypto communications module coupled to said crypto engine **(Fig. 7, Numeral 326, data link and other links that are connected to component 326 providing data and control signals)**; and

said PHY communications module being operatively coupled to said crypto communications module **(Fig. 7, encoder/scrambler is residing within PHY and sharing control signals with other components of PHY).**

Regarding **claim 2**, the rejection of claim 1 is incorporated and further Fujimori discloses that PHY communications module is configured to provide connectivity through a MDIO/MDC interface **(Fig. 7, Numerals 380A and 380, also at paragraph 0035, "The MAC 20 also interfaces to the single-chip multi-sublayer PHY 10**

through the serial MDIO (management data input/output) interface 16."), and said PHY controls the operation of said crypto device **(Fig. 7, Numeral 326 and 316)**

Regarding **Claim 4**, the rejection of claim 1 is incorporated and further Fujimori discloses that PHY communications module is configured to provide connectivity through a MDIO/MDC interface **(Fig. 7, Numerals 380A and 380, also at paragraph 0035, "The MAC 20 also interfaces to the single-chip multi-sublayer PHY 10 through the serial MDIO (management data input/output) interface 16.")**; and said crypto communications module is coupled to said MDIO/MDC interface **(Fig. 7, numerals 312, 380, 380A, 326, Paragraph 0082, Incoming data through component 312, which goes through scrambler, relay on the clock signal from MDC/MDIO interface, therefor scrambler can be seen coupled to MDIO/MDC interface.)**

Regarding Claim 5, the rejection of claim 1 is incorporated and further Fujimori discloses a master communications module coupled between said PHY communications module and said crypto communications module **(Fig. 7, "Management & Control Block")**

Regarding Claim 6, the rejection of claim 1 is incorporated and further Fujimori discloses that crypto communications module is configured to provide connectivity through a MDIO/MDC interface **(Fig. 7, numerals 312, 380, 380A, 326, Paragraph 0082, Incoming data through component 312, which goes through scrambler, relay on the clock signal from MDC/MDIO interface, therefor MDIO/MDC interface can be seen as an interface that enables data to go to the scrambler component.)**, and said crypto device controls the operation of said PHY **(Fig. 7, Numeral 326, data**

that goes through PHY passes through encoder/scrambler therefor encoder/scrambler component infect controls the operation of PHY)

Regarding **Claim 7**, the rejection of claim 1 is incorporated and further Fujimori discloses that PHY communications module is configured to provide connectivity through a serial wire interface **(Fig. 4, Numeral 19, Paragraph 0035, "The single-chip multi-sublayer PHY 10 also interfaces to EEPROM 40 through a two-wire serial interface 19")**

Regarding **Claim 8**, the rejection of claim 7 is incorporated and further Fujimori discloses that serial wire interface is configured to communicate with a plurality of devices **(Fig. 7, numeral 382, 383, Paragraph 0084, "The single-chip 10 2-wire serial interface 19 accesses the external devices through two dedicated interface signals, SDA (data) 383 and SCL (clock) 382.")**

Regarding **Claim 9**, the rejection of claim 8 is incorporated and further Fujimori discloses that plurality of devices include at least one device that communicates at the PHY level **(Fig. 7, SDA (data) 383 and SCL (clock) 382)** and at least one device that performs security functions **(Fig. 7, Numeral 382, SCL (Clock)).**

Regarding **Claim 10**, the rejection of claim 7 is incorporated and further Fujimori discloses that serial wire interface communicates with at least one device that performs both PHY and Security functions **(Fig. 7, Numeral 382, SCL (Clock))**.

Regarding **Claim 11**, Fujimori discloses an apparatus for providing link layer security in a Physical Layer Transceiver (PHY) comprising:

analog circuitry means for providing connectivity to a data transmission medium **(Fig. 4, Numerals 1, 17 and 30 and paragraph 0030)**

digital circuitry means coupled to said analog circuitry means **(Fig. 5, Numeral 130)**, said digital circuitry providing connectivity to a Media Access Controller (MAC); **(Fig. 5, numerals 20 and 10)** PHY communications means coupled to said analog and digital circuitry means **(Fig. 4, Numerals 15 and 17);**

crypto engine means coupled to said digital circuitry means **(Fig. 7, Numeral 326, "Encoder/Scrambler")**;

crypto communications means coupled to said crypto engine means **(Fig. 7, Numeral 326, data link and other links that are connected to component 326 providing data and control signals)**; and

said PHY communications means being operatively coupled to said crypto communications module **(Fig. 7, encoder/scrambler is residing within PHY and sharing control signals with other PHY devices).**

Regarding **claim 12**, the rejection of claim 11 is incorporated and further Fujimori discloses PHY communications means being configured for providing connectivity through a MDIO/MDC interface **(Fig. 7, Numerals 380A and 380, also at paragraph 0035, "The MAC 20 also interfaces to the single-chip multi-sublayer PHY 10 through the serial MDIO (management data input/output) interface 16.")**, and said PHY controls the operation of said crypto device **(Fig. 7, Numeral 326 and 316)**

Regarding **Claim 14**, the rejection of claim 11 is incorporated and further Fujimori discloses PHY communications means is configured to provide connectivity through a

MDIO/MDC interface **(Fig. 7, Numerals 380A and 380, also at paragraph 0035, "The MAC 20 also interfaces to the single-chip multi-sublayer PHY 10 through the serial MDIO (management data input/output) interface 16.")**; and said crypto communications means is coupled to said MDIO/MDC interface **(Fig. 7, numerals 312, 380, 380A, 326, Paragraph 0082, Incoming data through component 312, which goes through scrambler, relay on the clock signal from MDC/MDIO interface, therefor scrambler can be seen coupled to MDIO/MDC interface.)**

Regarding Claim 15, the rejection of claim 11 is incorporated and further Fujimori discloses a master communications means coupled between said PHY communications means and said crypto communications means **(Fig. 7, "Management & Control Block")**

Regarding Claim 16, the rejection of claim 11 is incorporated and further Fujimori discloses that crypto communications means is configured to provide connectivity through a MDIO/MDC interface **(Fig. 7, numerals 312, 380, 380A, 326, Paragraph 0082, Incoming data through component 312, which goes through scrambler, relay on the clock signal from MDC/MDIO interface, therefor MDIO/MDC interface can be seen as an interface that enables data to go to the scrambler component.)**, said crypto device means controls the operation of said PHY **(Fig. 7, Numeral 326, data that goes through PHY passes through encoder/scrambler therefor encoder/scrambler component infect controls the operation of PHY)**

Regarding **Claim 17**, the rejection of claim 11 is incorporated and further Fujimori discloses that said PHY communications means is configured to provide connectivity through serial wire interface means **(Fig. 4, Numeral 19, Paragraph 0035, "The single-chip multi-sublayer PHY 10 also interfaces to EEPROM 40 through a two-wire serial interface 19")**

Regarding **Claim 18**, the rejection of claim 17 is incorporated and further Fujimori discloses that said serial wire interface means is configured to communicate with a plurality of devices **(Fig. 7, numeral 382, 383, Paragraph 0084, "The single-chip 10 2-wire serial interface 19 accesses the external devices through two dedicated interface signals, SDA (data) 383 and SCL (clock) 382.")**

Regarding **Claim 19**, the rejection of claim 18 is incorporated and further Fujimori discloses that said plurality of devices include at least one device that communicates at the PHY level, **(Fig. 7, SDA (data) 383 and SCL (clock) 382)** and at least one device that performs security functions **(Fig. 7, Numeral 382, SCL (Clock)).**

Regarding **Claim 20**, the rejection of claim 17 is incorporated and further Fujimori discloses that said serial wire interface communicates with at least one device that performs both PHY and Security functions. **(Fig. 7, Numeral 382, SCL (Clock)).**

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Dhir et al. (US 2005/0084076 A1): Discloses wireless transceiver in which field programmable gate array (FPGA) is coupled to memory having programming instructions for configuring the FPGA with a medium access layer selected from more than one type of medium access layers. A physical layer is hardwired or embedded on the FPGA, or a separate integrated circuit for the physical layer is used. This device provides link layer security by having authentication and encryption functionalities on FPGA.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh Paliwal whose telephone number is (571) 270-1807. The examiner can normally be reached on M-F: 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian P. Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YP
4/25/2007

BRIAN WERNER
SUPERVISORY PATENT EXAMINER